**CLAIM AMENDMENTS:**

1. (currently amended): A semiconductor device comprising:

a semiconductor chip having a first main surface on which a plurality of electrode pads are provided, a second main surface which opposes said first main surface, and a plurality of side surfaces positioned between said first main surface and said second main surface;

an extension portion formed in contact with said side surfaces of said semiconductor chip so as to surround said semiconductor chip;

an insulating film formed on a surface of said extension portion and said first main surface such that a part of each of said electrode pads is exposed;

a plurality of wiring patterns formed on said insulating film so as to be electrically and directly connected to said electrode pads, respectively and extended from said electrode pads to the surface of said insulating film on said extension portion and said first main surface;

a plurality of electrode posts formed on said wiring patterns so as to be electrically and directly connected therewith;

a sealing portion formed on said wiring patterns and said insulating film such that the top surface of said electrode posts is exposed; and

a plurality of external terminals provided on the top surface of said electrode posts in a region including the upper side of said extension portion;

wherein the electrode pads are arranged in a first line extending in a first direction along a peripheral edge of the semiconductor chip on the first main

surface, and the external terminals are arranged in a second line extending in a second direction perpendicular to said first direction, and are electrically ~~and directly~~ connected to the electrode pads in a one-on-one connection relationship.

2. (canceled).

3. (original): The semiconductor device according to claim 1, wherein said electrode posts are formed from a conductive material.

4. (previously presented): The semiconductor device according to claim 3, wherein a thin oxidation layer is formed on a side surface of said electrode posts.

5. (original): The semiconductor device according to claim 1, wherein said external terminals are formed as solder balls.

6. (original): The semiconductor device according to claim 1, wherein said external terminals are lands.

7. (previously presented): The semiconductor device according to claim 1, wherein a portion of said wiring patterns on a boundary and a vicinity of a boundary between a region on the upper side of said semiconductor chip and said

extension portion is formed wider or more thickly than other portions of said wiring patterns.

8. (original): The semiconductor device according to claim 1, wherein said extension portion is formed from a material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

9. (original): The semiconductor device according to claim 8, wherein said extension portion is formed from a liquid resin having a linear expansion coefficient in a lower temperature range than glass transition temperature of less than $1.5 \times 10^{-5}$/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.

10. (withdrawn): The semiconductor device according to claim 1, comprising:

a passive element comprising connection terminals and provided on said extension portion; wherein

the insulating is film formed such that a part of said connection terminals is exposed.

11. (withdrawn): The semiconductor device according to claim 10, wherein a portion of said wiring patterns on a boundary and a vicinity thereof between a

region on the upper side of said semiconductor chip and said extension portion is formed wider or more thickly than other portions of said wiring patterns.

12. (withdrawn): The semiconductor device according to claim 10, wherein said passive element provided on said extension portion comprises a plurality of connection terminals, one of said connection terminals being connected to said electrode pads and the other connection terminal being connected to said external terminals.

13. (withdrawn): The semiconductor device according to claim 10, wherein said passive element provided on said extension portion comprises a plurality of connection terminals, one of said connection terminals being connected to a specific external terminal and the other connection terminal being connected to a different external terminal.

14. (withdrawn): The semiconductor device according to claim 10, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals, wherein said sealing portion is formed such that the top surface of said electrode posts is exposed.

15. (withdrawn): The semiconductor device according to claim 10, wherein said electrode posts are formed from a conductive material.

16. (withdrawn): The semiconductor device according to claim 10, wherein a thin oxidation layer is formed on a side surface of said electrode posts.

17. (withdrawn): The semiconductor device according to claim 10, wherein said external terminals are solder balls.

18. (withdrawn): The semiconductor device according to claim 10, wherein said external terminals are lands.

19. (withdrawn): The semiconductor device according to claim 10, wherein said extension portion is formed from a material having a greater molding shrinkage than the molding shrinkage of said sealing portion.

20. (withdrawn): The semiconductor device according to claim 19, wherein said extension portion is formed from a liquid resin having a linear expansion coefficient in a lower temperature range than glass transition temperature of less than $1.5 \times 10^{-5}$/°C and a modulus of elasticity within a range of 7.8 to 22 GPa.